corresponding I/O pad **12**. Thus, during the low-power mode of operation, the respective states of the I/O pads **12** are retained.

[0028] Microcontroller **10** can be caused to wake up and return to the active mode, for example, when an internal counter reaches a predetermined count or by a reset signal. Power state management unit **16** then releases the "Core_is_on" signal (i.e., by driving a logical zero ("0") on line **26**), and control of the input signals (i.e., "Input data," Output enable" and "Drive strength control") returns to I/O controller **18**. As a result, the input signals (i.e., "Input data," Output enable" and "Drive strength control") would return, for example, to their default states.

[0029] Further details of the user-controlled, programmable mode of operation for the pad state retention function are illustrated in FIGS. **5** and **6**. As explained above, the user can enable the pad retention function by writing a logical one ("1") to pad retention enable register **40** (see FIG. **5**). Writing a logical one ("1") to pad retention enable register **40** overrides the signal from power state management unit **16** on line **26** and causes the "Core_is_on" signal at the output of NOR gate **22** to drop to a logical low value. With the "Core_is_on" signal at a logical low value, the states of the input control signals (i.e., "Input data," Output enable" and "Drive strength control") are retained by a respective set of latches **32**, **34**, **36**. As shown in FIG. **6**, this should be done before placing microcontroller **10** into the power save mode so that the control signals for retaining the states of I/O pads **12** are latched before microcontroller **10** enters the low-power mode. After microcontroller **10** wakes up and returns to the active mode, the user can release the pad state retention function by writing a logical zero ("0") to pad retention enable register **40**. As the release occurs in this case through software, a small delay may be introduced. Such a small delay can be advantageous. For example, upon waking up, the pad retention preferably should be released through software control only after I/O controller **18** is properly configured (e.g., to ensure that "Input data," Output enable" and "Drive strength control" signals are the same as they were prior to entering the low-power mode). Such operation can help ensure that I/O pads **12** have the same value during the entire I/O pad sequence (e.g., active mode>>>shutdown mode>>>active mode).

[0030] In some implementations, it may be desirable to include isolation cells, such as logical AND gates, between the core logic (i.e., I/O controller **18**) and I/O connector state control logic **20**. Providing such isolation cells can help ensure that signals from the powered-down domain do not propagate to and from the pad logic interface.

[0031] Other implementations are within the scope of the claims.

1. (canceled)

2. A microcontroller operable in a low-power mode, the microcontroller comprising:

a plurality of I/O connectors;

an I/O controller operable to provide control signals for controlling states of the I/O connectors, wherein the I/O controller is powered off or deactivated during the low-power mode; and

I/O connector state retention logic operable to store states of the control signals so as to maintain the I/O connectors in respective states that existed just prior to the I/O controller becoming powered off or deactivated, wherein the states are maintained while the microcontroller is in the low-power mode.

3. The microcontroller of claim **2** wherein the I/O connectors include at least one of I/O pads or I/O pins.

4. The microcontroller of claim **2** wherein the I/O connector state retention logic includes latches.

5. The microcontroller of claim **4** wherein the latches are SR latches.

6. The microcontroller of claim **4** wherein the latches are operable to be enabled to retain input data values for the I/O connectors even after the microcontroller enters the low power mode.

7. The microcontroller of claim **4** wherein the latches are operable to be enabled to retain output enable values for the I/O connectors even after the microcontroller enters the low power mode.

8. The microcontroller of claim **4** wherein the latches are operable to be enabled to retain drive strength control values for the I/O connectors even after the microcontroller enters the low power mode.

9. The microcontroller of claim **2** wherein the I/O connector state retention logic is operable to retain input data values, output enable values and drive strength control values for the I/O connectors even after the microcontroller enters the low power mode.

10. The microcontroller of claim **9** operable to return to an active mode from the low-power mode, wherein, in the active mode, control of input signals for the input data values, output enable values and drive strength control values returns to the I/O controller.

11. The microcontroller of claim **10** operable to return to the active mode from the low-power mode when an internal counter reaches a predetermined count.

12. The microcontroller of claim **10** operable to return to the active mode from the low-power mode in response to a reset signal.

13. The microcontroller of claim **2** wherein at least some of the control signals for controlling states of the I/O connectors allow the I/O controller to drive a logical 1 or 0 onto the I/O connectors.

14. The microcontroller of claim **2** wherein at least some of the control signals for controlling states of the I/O connectors indicate whether the I/O pads are to be used for input or output.

15. The microcontroller of claim **14** wherein if a particular one of the control signals indicates that a particular one of the I/O pads is to be used for output, the particular control signal also enables an output buffer.

16. The microcontroller of claim **2** wherein at least some of the control signals for controlling states of the I/O connectors indicate a drive strength setting.

17. A microcontroller operable in a low-power mode, the microcontroller comprising:

a plurality of I/O connectors;

an I/O controller operable to provide control signals for controlling states of the I/O connectors, wherein the I/O controller is powered off or deactivated during the low-power mode;

I/O connector state retention logic operable to store states of the control signals so as to maintain the I/O connectors in respective states that existed just prior to the I/O controller becoming powered off or deactivated, wherein the states are maintained while the microcon-